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# Low Voltage Time-Resolved Emission (TRE) Measurements of VLSI Circuit

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**Abstract:** Advanced technology nodes with small feature sizes and increased design complexity make it increasingly time-consuming to determine the root cause of yield loss. Several of the defects also occur inside a circuit making physical failure analysis (PFA) and electrical failure analysis (EFA) much more challenging. EFA has been instrumental in driving product yield and reliability for consumer products such as mobile phones and computer chips. It involves the use of state-of-the-art tools and techniques. One of the main changes EFA analyses is an enhancement of dynamic EFA in circuit failed in functional test. We propose a technique for advanced Electrical Failure Analysis (EFA) tool with a Superconducting Nanowire Single Photon Detector (SnSPD) system and its application to low voltage Time-Resolved Emission (TRE) measurements (also known as Picosecond Imaging Circuit Analysis, PICA) of scaled VLSI circuits with enhanced sensitivity for discussing Time Resolved Emission (TRE). In order to understand the figures of advantage that a single-photon detector should have to enable the acquisition of time resolved emission waveforms for low voltage applications. We will provide that measurements down to a low 1 V supply voltage were made possible by a careful optimization of the detector front-end electronics. We also characterized the emission from devices with different threshold voltages in order to understand how the emission contributions depend on this parameter and how this affects the resulting waveform. we hope to be able to show soon even better results that should allow continued application of the non-invasive TRE and PICA technology towards future scaled nodes with smaller gates and lower supply voltages.

**Keywords:** PICA, TRE, Functional, EFA

## 1. Introduction

Time-Resolved Emission (TRE) measurement, is known as Picosecond imaging circuit analysis (PICA), based on A collection of near-infrared light (NIR) emitted by a hot source Carriers in transistor channels are an invaluable method Widely adopted for testing and failure analysis field. This technology can be detected non-invasive Probe switching activity inside VLSI circuits for measurements Skew, propagation delay, duty cycle, etc. [1-9]. In recent the years, its capabilities have been continuously expanded.

Use of light due to off-state leakage current (LEOSLC) [10-15] Apply to brand new applications, such as Logic state mapping [10], mode debugging [12], latch Ignition study [16, 17], power supply noise [14, 18, 19] and Slew rate measurement [20], self-heating estimation [21], System and random device variability characterization [15], security and counterfeit detection for ICs [22], etc.

Continuing trends in the semiconductor industry for smaller devices and lower supply voltages [23] causes major changes in intensity and spectrum light from IC [24]: detectable light decreases is exponentially related to the electric field in the transistor, and it has a linear relationship with the lateral dimension of the CMOS. In addition, a decrease in circuit voltage also results in longer wavelengths of the spectral distribution of the emitted light.

For these reasons, the detectors have higher sensitivity at these longer wavelengths, as well as lower intrinsic noise (dark counts), are needed.

In recent years, advances in the understanding of the detector physics, material fabrication processes, lithography, and cryogenic cooling technology have allowed the manufacture of significantly better SnSPDs, detectors and systems, that promise significant improvements for TRE applications in VLSI testing [25-27].

In this paper, we will discuss the performance of a

Single-Photon Detector that system developed by GPM (Gallant Precision Machining).

## 2. Experiment

### *2.1. Design Architecture*

Custom-designed test chip manufactured using 32 nm low power technology was used to characterize PICA (SnSPD) detector. The chip contains many designed experiments such as delay lines, PLLs, scan chains, and other circuits. In terms of size and pitch, the chip can perform general evaluations of detector sensitivity, jitter, and lateral spatial resolution, respectively.

For the purposes of this paper, most of the data has been collected from dedicated inverter-based delay line.

An example of optical emission from an operating CMOS. The switching transitions generate optical emission from hot carriers. The timing and relative strength of the emission is shown schematically for a simple inverter in Figure 1.

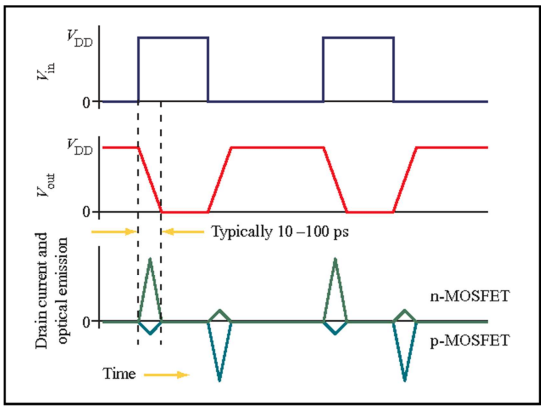


***Figure 1.*** *Schematic of the relationship between electrical and hot carrier induced optical emission waveforms for a CMOS inverter.*

The dominant emission will be associated with nFETs undergoing to zero transitions. The presence of current in n- and pFETs is necessary for observable light emission, but its emission cannot be guaranteed because the presence of hot carriers in the FET depends on both the source-drain voltage and the gate voltage.

### *2.2. Characterization of the SnSPD System*

Initial characterization of the system, consisting of the SnSPD and optics with a 50X lens, showed good performance. The jitter of the system during a real measurement (which includes the circuit, pulse generator, timing electronics, and detector jitter) was shown to be less than 145 ps-FWHM shown in Figure 2. For a typical bias current of 19 uA used in our experiments, the intrinsic DCR (dark count rate) of the detector was also measured to be below 10 cps (thousand counts per second) in free running conditions shown in Figure 3.

### *2.3. Low Voltage Circuit Measurement*

To simplify the analysis, a simple inverter with a 5 x 120 nm CMOS, switching at a fixed 15.625 ns (64 MHz) period was used in Figure 4. The timing electronics was setup for a 125ns trigger loop. Figure 5 shows the first TRE waveform obtained from an CMOS when the power supply voltage is set to 1.5 V, it is 1 minute in this case collect, then 8X periodic folding, and low-pass filtering for clear identification switching emission peak corresponding to falling edge by N-MOS and P-MOS, as well as the low and high LEOSLC regions of the waveform.

Figure 6 shows an example of a 10 min TRE waveform acquired from the same inverter gate at 1 V, the reduction 33% voltage as presented for a TRE waveform.

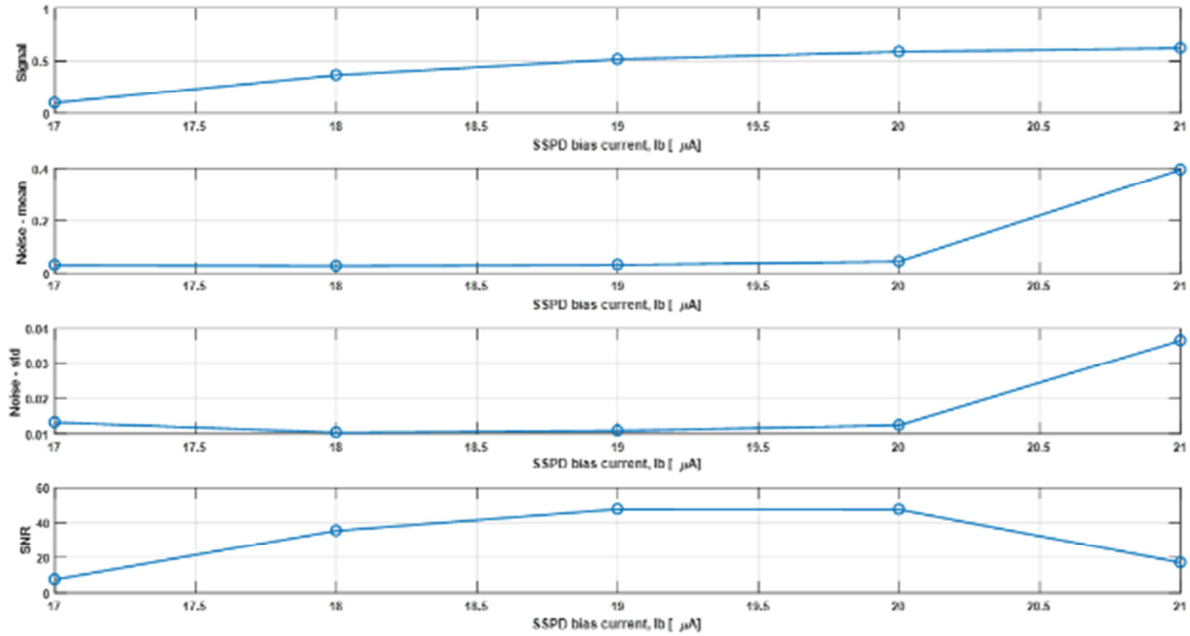


***Figure 2.*** *SnSPD system bias current performance during operation.*

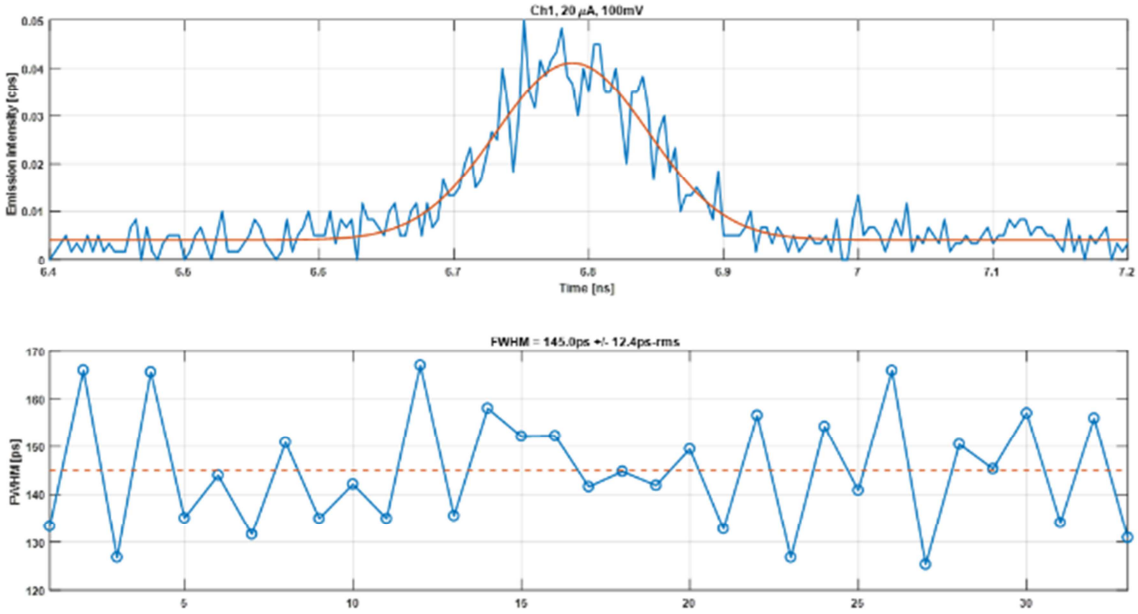


***Figure 3.*** *SnSPD system Jitter performance during operation.*

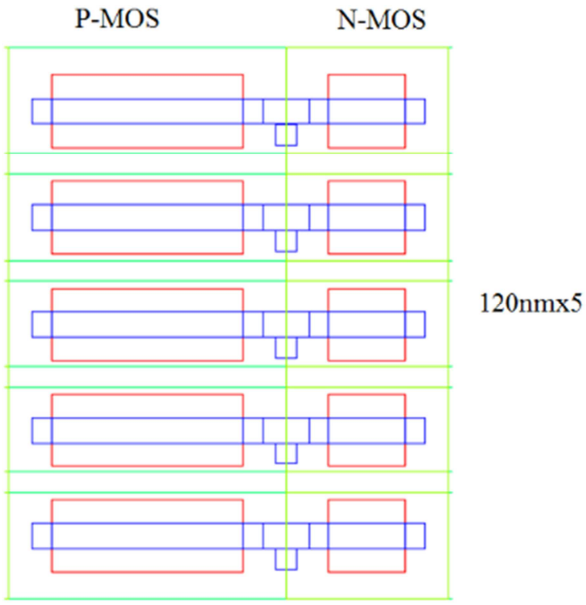


***Figure 4.*** *Inverter gate layout used for the TRE measurements.*

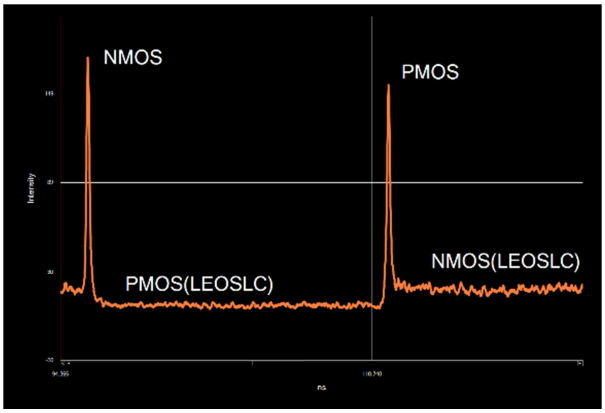


***Figure 5.*** *1.5 V TRE waveform acquired in 1 min.*

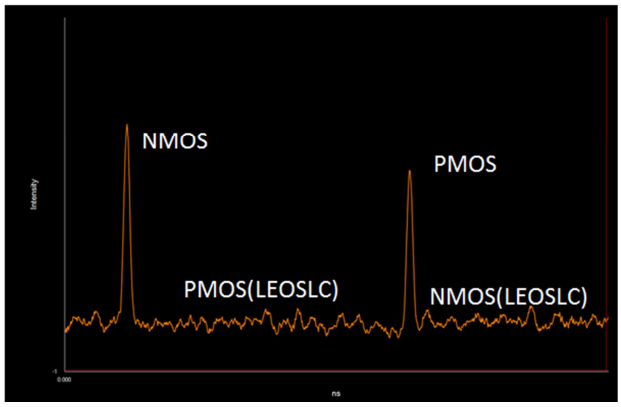


***Figure 6.*** *1 V TRE waveform acquired in 10 min.*

### *2.4. Propagation Delay Measurements at Low Voltage*

To demonstrate the basic function of the PICA system in actual PICA measurements, the signal propagation delay along the inverter chain described in Figure 3 was measured at nominal 1.5 V and reduced 1.25 V.

Figure 7 (a) shows an zoom in view of the switching transition events along the odd-numbered gates of the inverter chain at 1.5 V. The result was collected in 3 minutes using a 15.625 ns (64 MHz) clock and a 125ns trigger loop. The switched emission peaks are fitted to a low-pass filter and Gaussian, respectively, and the calculated centroids are reported in Figure 7 (b). A gate propagation delay of ~5.7 ps and ~8.4 ps are estimated for 1.5V and 1.25 V conditions, respectively.

### *2.5. n-FET vs. p-FET Signal Strength*

The ratio of switching emission signal strength from n-FETs and p-FETs has changed significantly over the years, with the p-FET / n-FET usually becoming closer to one. Although the ratio is a strong function of the technology node, drain engineering, process parameters, and specific PICA detector,

we decided to perform a qualitative evaluation experiment using the same gate discussed in the low v*oltage experiment in Figure* 3. Separated measurements were acquired for the same test conditions from both the n-FET and p-FET of the same inverter by focusing the collection spots at different physical locations. As a consequence, the p-FET / n-FET emission ratio is found to be substantially independent of the circuit supply voltage as shown in Figure 8.

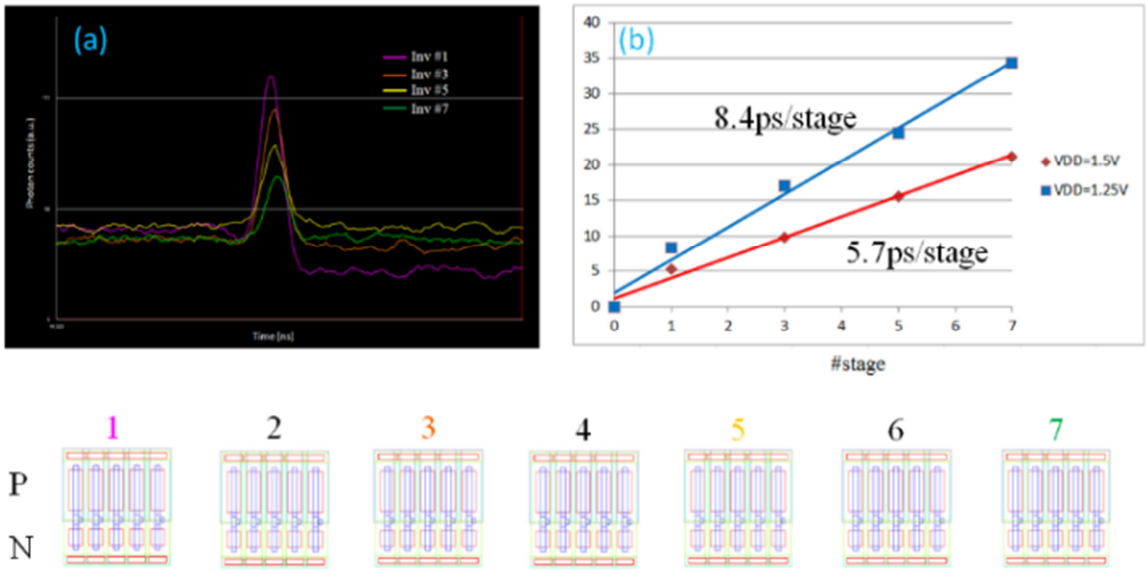


***Figure 7.*** *(a) TRE waveforms at different position along a delay line and (b) calculated propagation delay.*

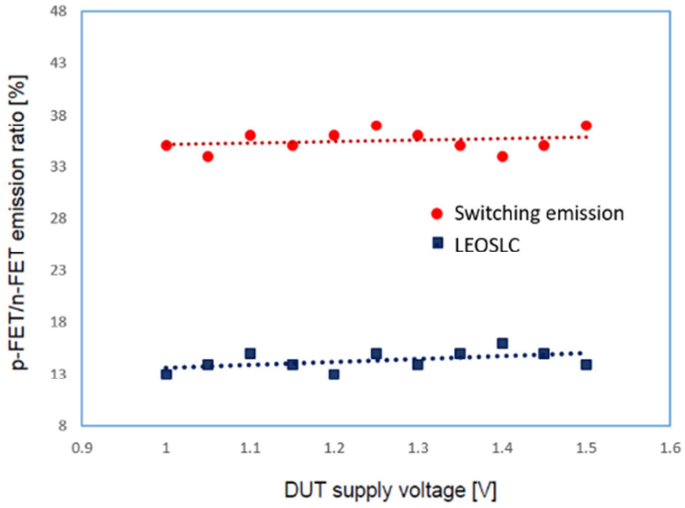


***Figure 8.*** *p-FET / n-FET emission ratio for both switching emission and LEOSLC.*

## 3. Conclusion

In this paper, we propose a novel time-resolved emissions (TRE) system and its application in low-voltage measurement to scale VLSI circuits.

We will demonstrate TRE measurements down to 1V in commercial tools.

In fact, this is the limiting factor in system sensitivity when operating the chip at low voltage. Thanks to the optimization of the electronic equipment used with the addition of the detector, we can obtain the TRE waveform from a 32 nm chip with an operating voltage of 1 V within 10 minutes. As far as we know, it proves how this truly non-intrusive testing technique can be used in future technologies and reduces the power supply voltage. Meanwhile, it is found that the p-FET/n-FET emission ratio is independent of the circuit power supply voltage.

There are still two main concerns remain: sensitivity and spatial resolution. The TRE signal decays exponentially (~2X / 100mV) by the lowering supply voltage and the diffraction-limited collection spot is intrinsically larger than laser-based techniques due to the longer wavelength involved.

TRE can still be effectively used to detect circuit signals at lower magnifications or with air gap lenses. Ultimately, applications, specific failure mechanisms, tool availability, user experience, the data analysis software package can

determine which tool is suitable and more effective for each test case.

We hope to show better results as soon as possible so that non-invasive TRE and PICA technologies can continue to be applied to future expansion nodes with smaller gates and lower supply voltages.

Significant improvements coming in the future:

1. Microscope with extended spectral response
2. Studied how the emission components change in case of devices with different threshold voltages.
3. Developed SIL with higher N. A.(spatial resolution)
4. New SnSPD with higher sensitivity

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